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FACSIMILE TRANSMITTAL

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FROM: Steven M. Jensen

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Our Docket No.: 56956 (71987)

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Re: U.S. Serial Number 10/075,043

MESSAGE:

Please enter the attached Response to Office Action.

Docket No. 56956 (71987)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:	D. Tseng et al.		
U.S. SERIAL NO.:	10/075,043	GROUP:	2823
FILED:	February 12, 2002	EXAMINER:	K. Nguyen
FOR:	METHOD AND SYSTEM OF WIRE BONDING FOR USE IN FABRICATION OF SEMICONDUCTOR PACKAGE		

CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted by facsimile to Group 2800 of the U.S. Patent & Trademark Office by facsimile number 703-872-9318 on December 24, 2003.

By: _____
Steven M. Jensen

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

RESPONSE TO OFFICE ACTION

Applicants are in receipt of the Office Action dated September 25, 2003 of the above-referenced application. Applicants respond to the Office Action as follows.

Applicants' claimed invention is directed to a method and system of wire bonding for use in semiconductor package fabrication. As recited in claim 1, e.g., the claimed method includes steps of: preparing a substrate composed of a plurality of substrate units; providing a wire bonding station having a wire bonding mechanism and a testing mechanism; forming a plurality of bonding wires on one substrate unit of the substrate; introducing the wire-bonded substrate unit into the testing mechanism for performing an open/short (O/S) test, while forming bonding wires on a next adjacent substrate unit of the substrate, wherein if the test results indicate an open wire or short circuit, the testing mechanism generates a control signal to interrupt the wire bonding process.

With reference to FIG. 1, when one wire-bonded substrate unit of a substrate is introduced into a testing mechanism 12, a next adjacent substrate unit is simultaneously formed with bonding wires in a wire bonding mechanism 11. In the testing mechanism 12, the wire-bonded substrate unit is tested for wire bonding quality. If no open wires or short circuits occur, the wire-bonded substrate unit can be used for subsequent package fabrication. If wire opening or short-circuiting is detected, a control signal is generated to interrupt the wire-bonding process, and defective bonding wires are reworked (see specification at page 11, last paragraph to page 12, first paragraph).

Applicants' claimed invention can yield significant benefits. Because the testing mechanism is integrated with the wire bonding mechanism in the same wire bonding station, when an open/short test is performed on a wire-bonded substrate unit, the next substrate unit can be wire bonded simultaneously. If open wires or short circuits are detected on the wire-bonded substrate unit, the wire bonding mechanism can be stopped to allow the wire bonding mechanism to be repaired, thereby reducing fabrication costs, preventing batch production of inferior products, and enabling fabrication time to be shortened.

Claims 1-41 were rejected under 35 USC 103(a) as being unpatentable over U.S. Patent 6,204,074 to Bertolet et al. (hereinafter "Bertolet") in view of "the applicant's admitted prior art (AAPA)." This rejection is respectfully traversed.

With reference to claims 1, 12, 22, and 33, Bertolet and "AAPA," whether taken alone or in combination, fail to teach or suggest performing an open/short (O/S) test on one substrate unit while wire bonding a next adjacent substrate unit in the wire bonding station. Moreover, there is no teaching or suggestion of providing a wire bonding station having at least a wire bonding mechanism and a testing mechanism that are capable of performing an O/S test on one substrate unit of a substrate while simultaneously wire-bonding the next adjacent substrate unit.

Bertolet discloses a chip design process for fabricating a wire bonded and flip chip package, the process being provided for testing and burning in a semiconductor die without direct physical contact of the external testing device to the wire bond pad of the die (see, e.g.,

column 2, lines 49-63). FIG. 9 of Bertolet was cited in the Office Action allegedly to teach the O/S test performed in the Applicants' invention. However, Bertolet discloses a process for testing the *functionality* of the fabricated semiconductor die (see, e.g., column 14, lines 37-41), but does not teach or suggest performing an open/short (O/S) test to check the bonding wires.

As described above, the O/S test performed in the Applicants' invention is a test for checking whether the chip is wire-bonded to the substrate, but does not involve checking the functionality of the semiconductor die itself. Moreover, the testing mechanism in the Applicants' claimed invention is positioned adjacent the wire bonding mechanism in a wire bonding station, such that the O/S test is performed immediately after the wire-bonding step to check a substrate unit for any open wires or short circuits, prior to wire bonding the remaining substrate units. Bertolet does not teach or suggest at least these features of the Applicants' claimed invention.

As stated in the Office Action, "AAPA" was cited for teaching "forming bonding wires on a next adjacent substrate of the substrate simultaneously moved into the wire bonding mechanism" (Office Action, page 5). However, "AAPA" does not teach or suggest performing an open/short (O/S) test on one substrate unit while wire bonding a next adjacent substrate unit in the wire bonding station, as recited in claims 1, 12, 22, and 33.

As described on pages 3-4 of the application, according to the prior art process, an entire batch of substrates undergoes the wire-bonding step, and thereafter an O/S test is separately performed on the entire batch of substrates. As shown in FIG. 6 (PRIOR ART), a wire bonding process is performed on a batch of substrates (step 61). Then, the substrates are introduced into an O/S test machine (step 62), where the O/S test machine is separate from the wire bonding station. Therefore, according to the prior art system and process, the entire batch of substrates must be transferred to the O/S test machine before the next batch can be sent to the wire-bonding machine. As a result, defective substrates cannot be timely discovered before wire-bonding the next batch of substrates, making it difficult to uncover the sources of open wires or short circuits (see pages 3-4 of the specification). Applicants' claimed invention specifically addresses the deficiencies of the "AAPA," and provides a step of performing an open/short (O/S) test on one substrate unit while wire bonding a next adjacent substrate unit in the wire bonding station.

Even if "AAPA" were somehow combined with Bertolet, the combination would fail to teach or suggest the Applicants' claimed invention, for at least the reasons discussed above.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,

Date: December 24, 2003

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